Real-Time Digital Phase Demodulator for the ITER Toroidal Interferometer and Polarimeter (TIP)

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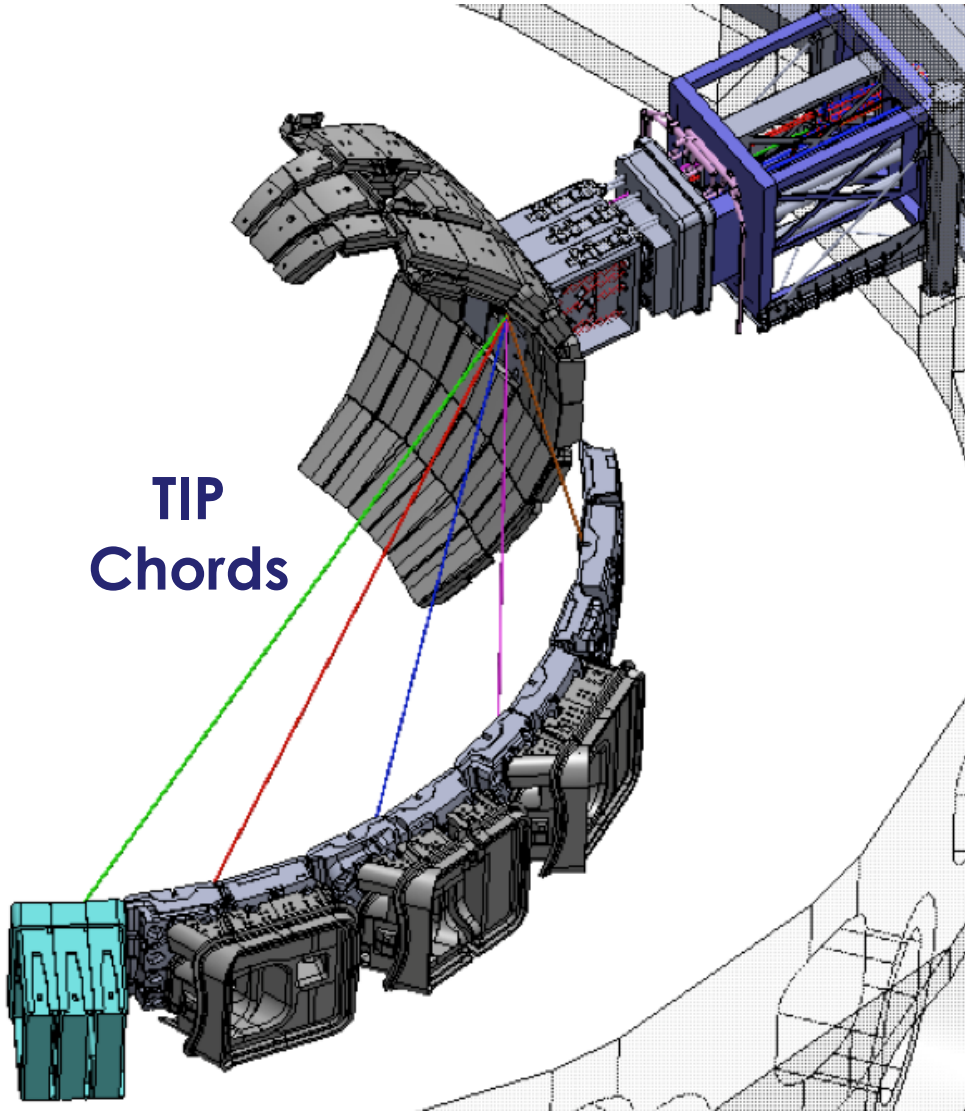
Abstract

The ITER TIP system requires real time phase demodulation of several radio-frequency (RF) signals to provide accurate electron density measurements essential for plasma control. This is accomplished using a four-channel digital phase demodulator (DPD) constructed using a high-density Field Programmable Gate Array (FPGA) coupled to high-speed analog-to-digital converters (ADC). The DPD samples signals from four optical detectors each containing frequencies at 4, 40, and 44MHz. Digital signal processing (DSP) techniques are used to separate the three frequencies and measure their phase. Two versions of DPDs have been constructed and tested on the DIII-D TIP system. The first was fabricated using a Xilinx Kintex-7 FPGA development board, a high-speed ADC module from Analog Devices, and custom hardware from Palomar Scientific Instruments. The second was assembled using ITER-approved components from National Instruments. The FPGA implementation for both versions was designed using Matlab System Generator and the VHDL programming language. Both systems have been shown to provide phase measurements with better than 0.01º accuracy at 500kHz bandwidth.

ITER Toroidal Interferometer and Polarimeter (TIP)

- A Primary Density Diagnostic
- Provides Real-Time line-integrated density measurements for feedback control of density
- Five tangential midplane chords
- Contributes to density profile reconstruction by constraining fits to Thomson scattering data
- Provides sensitive line-integrated measurements of density fluctuations from turbulence and coherent modes with frequencies into the MHz range

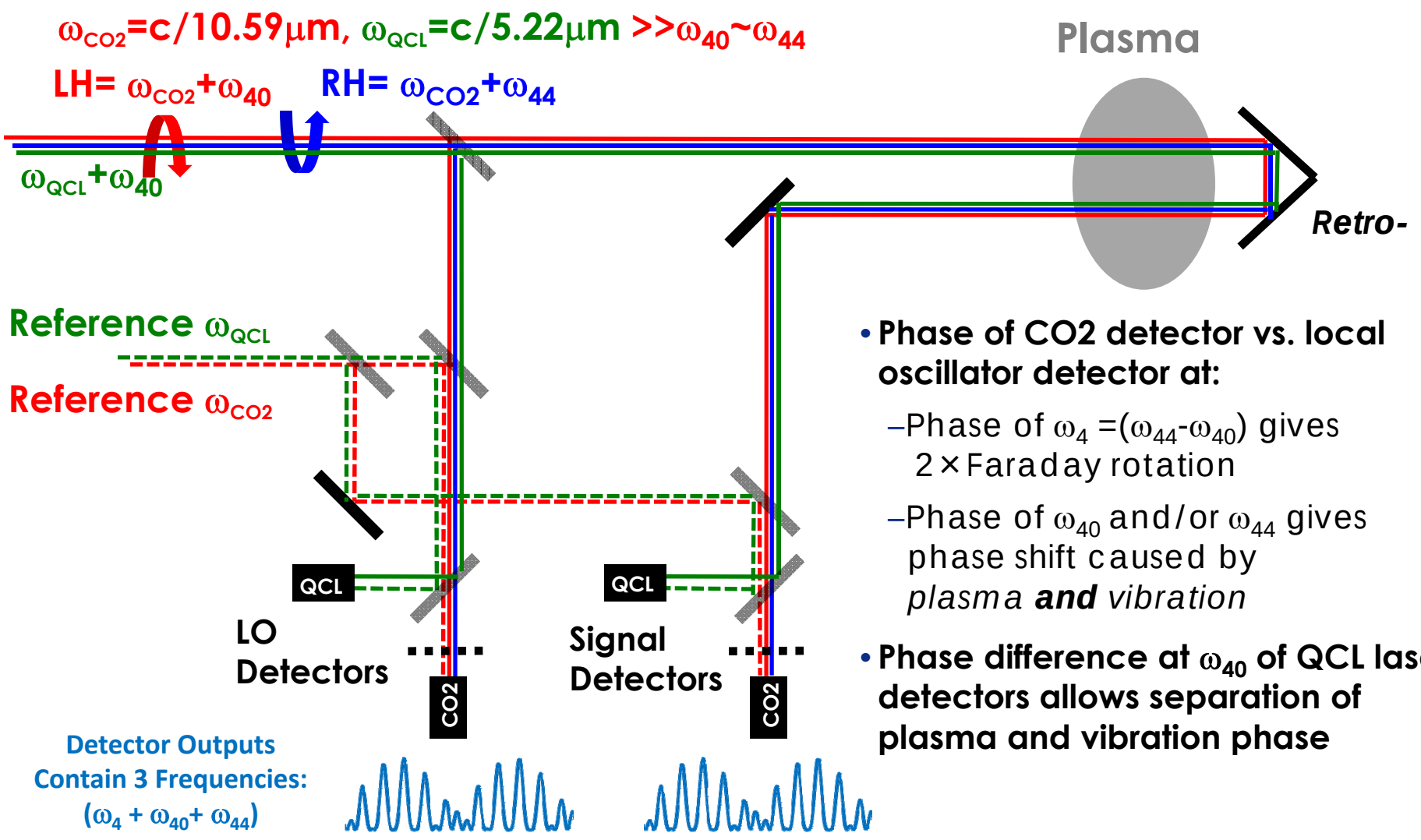


TIP Combines Two-Color Interferometer and Polarimeter

- **Utilizes a pair of heterodyned Mid-IR lasers**
  - Current design uses 10.6um (CO2) and 5.2um (QCL)
  - Acousto Optical Modulators (AOMs) are used to heterodyne the lasers at 40 and 44 MHz.
  - Each laser is detected at two places (four detectors)
  - Each detector contains 3 IF frequencies:
    - 40, and 44 MHz are Interferometer Signals
    - 4MHz is a mixing product containing Polarimeter Signal
- **Requires real time phase demodulation of each IF**
  - Phase measurements from each detector must be scaled, added, and subtracted
  - **Accuracy of .01° needed to meet ITER requirements**

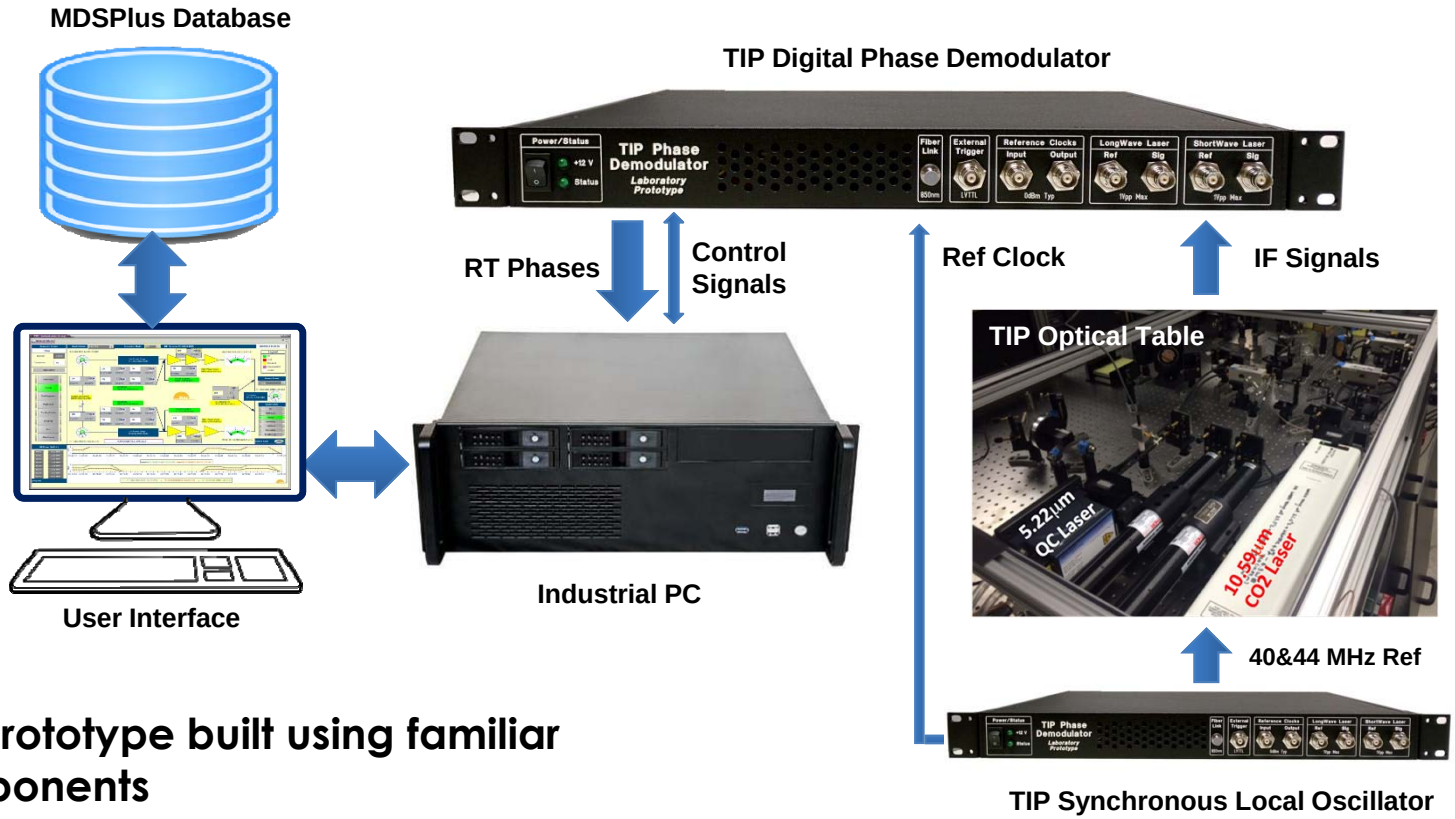
Typical detector signal containing 4, 40, and 44 MHz contributions

Polarimetry and Interferometry with Vibration Compensation



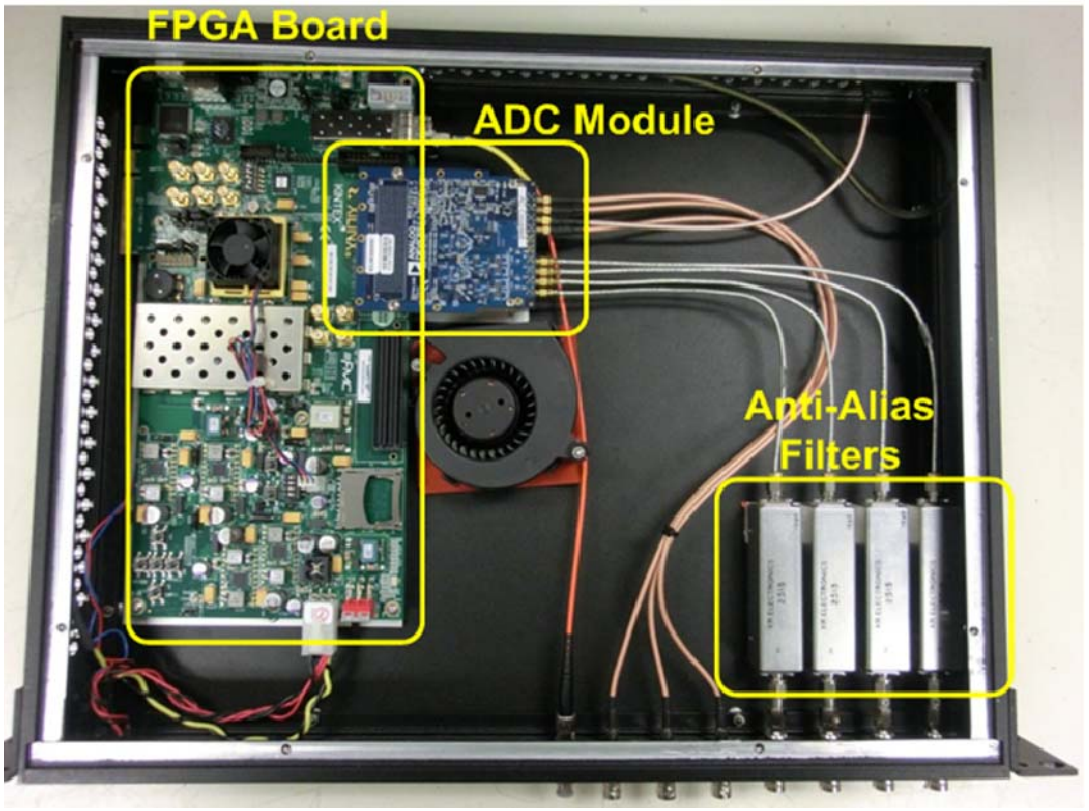
- **Phase of CO2 detector vs. local oscillator detector at:**
  - Phase of ω_4 =(ω_{44}-ω_{40}) gives 2×Faraday rotation
  - Phase of ω_{40} and/or ω_{44} gives phase shift caused by *plasma **and** vibration*
- **Phase difference at ω_{40} of QCL laser detectors allows separation of plasma and vibration phase**

Two Prototypes Built and Tested on DIII-D

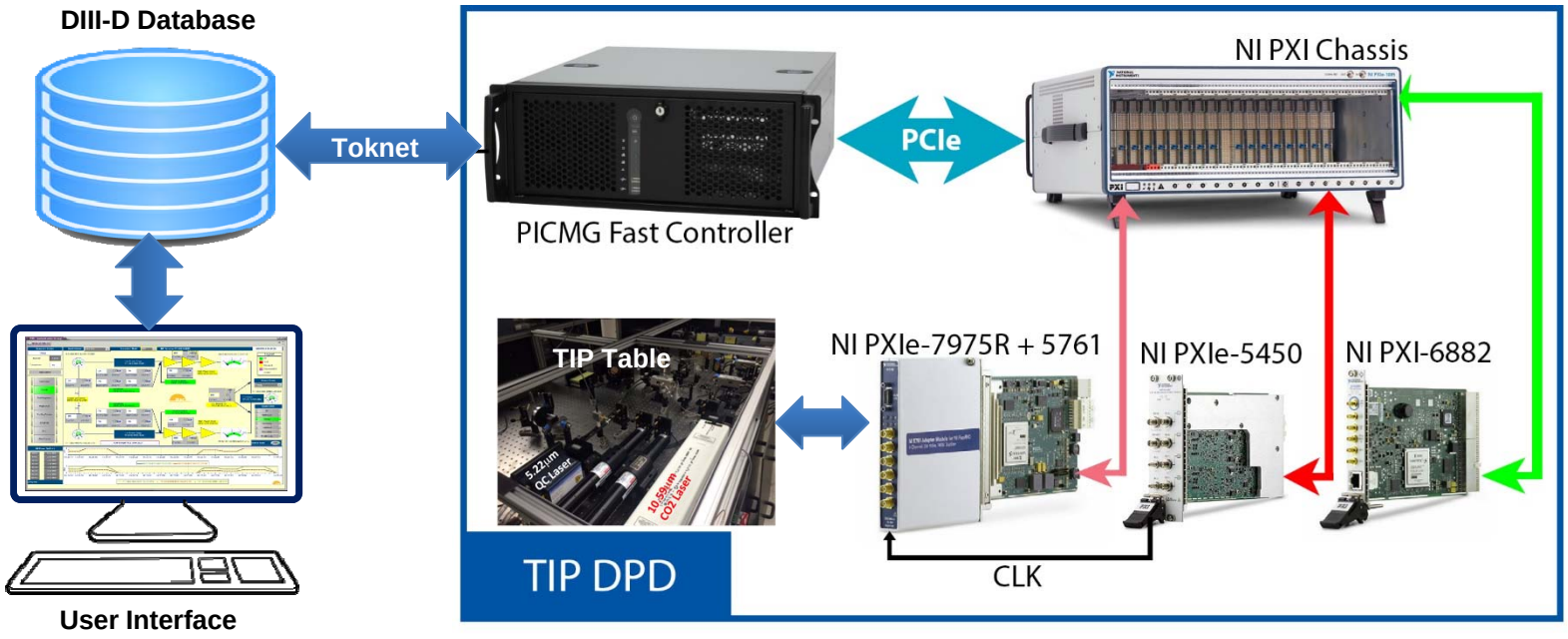


- First Prototype built using familiar components
- Second Prototype built using ITER-qualified components from *National Instruments*

First Prototype using KC705 Development Board

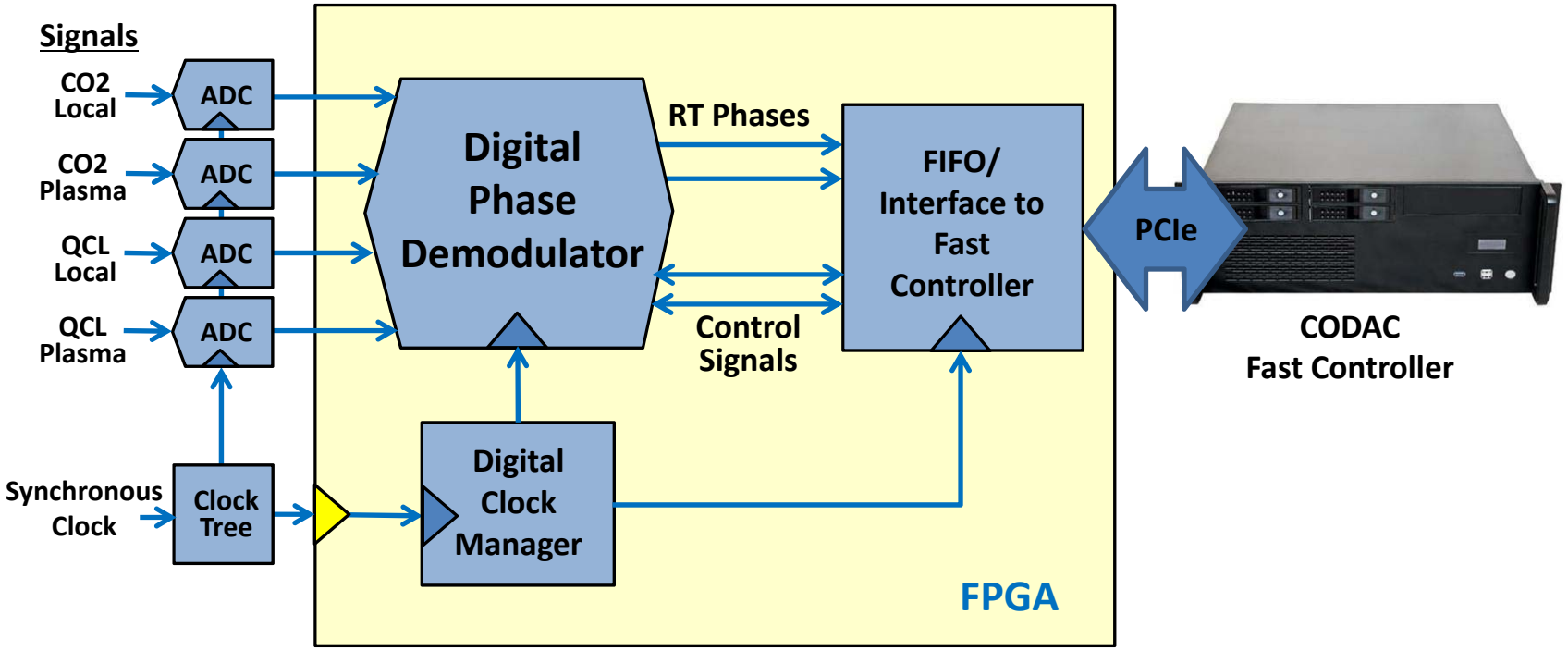


Second Prototype Uses ITER-Qualified Components



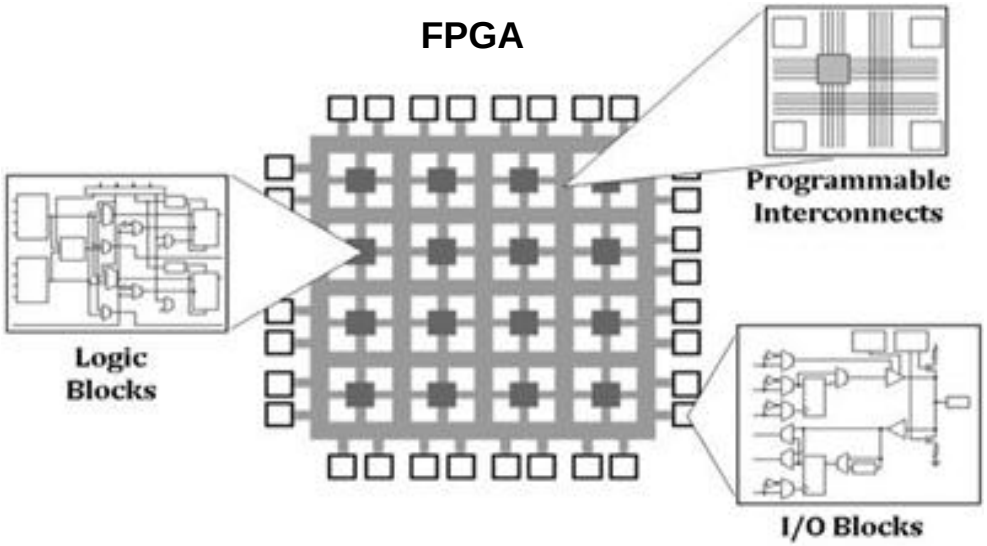
- **PXIe-based system created using components from *National Instruments***
  - NI PXIe-1062Q Chassis
  - NI PXIe-7975R FlexRIO FPGA
  - NI 5761 ADC Module
  - NI PXIe-5450 Signal Generator
  - NI PXIe-8381 Controller

Utilizes modern DSP, FPGA and ADC technologies



- **Four IF Signals are synchronously sampled using ADCs**
  - 160MSPS sampling rate, 16-bit
  - Sampling clock is synchronized with modulator source
- **Signals are processed using high-density FPGA**
  - Xilinx Kintex-7

What is an FPGA?



Field Programmable Gate Array

- Massive matrix of configurable logic gates and blocks
- Truly parallel in nature, rich in interconnect resources
- Extremely Fast and Flexible
- Ideal for DSP
- Programmed “In the Field” by external memory chip, device, or computer
- Sizes and families determine capability and cost

Quadrature Demodulation: *I* and *Q* Decomposition

A sinusoidal signal with magnitude *M*, frequency ω and phase ϕ can be decomposed into *In-phase* (*I*) and *Quadrature-phase* (*Q*) components:

$$V(t) = M\cos(\omega t - \phi) = I\cos\omega t + Q\sin\omega t$$

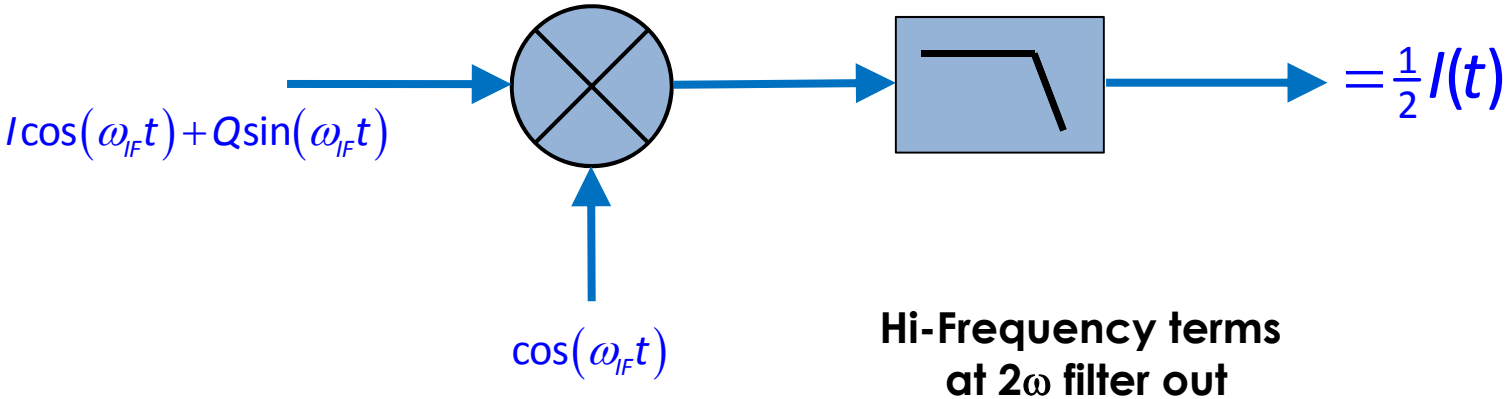
where

$$M^2 = I^2 + Q^2 \quad \text{and} \quad \phi = \tan^{-1}\left(\frac{Q}{I}\right)$$

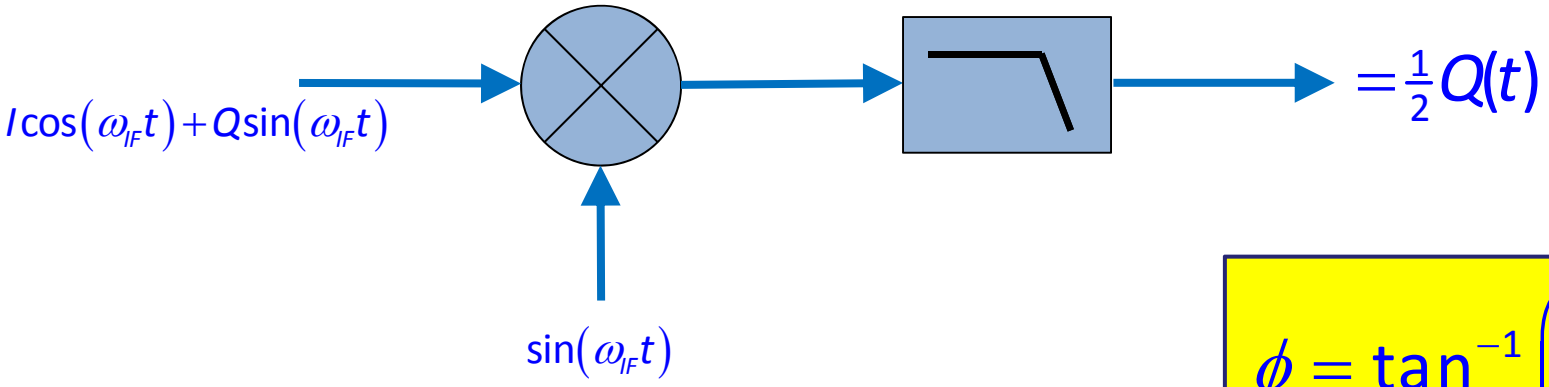
$I, Q,$ and ϕ vary with time

Quadrature Demodulation involves measuring *I* and *Q*.
***The Phase* ϕ is computed using the ATAN function**

Demodulation: In-phase and Orthogonal Signals

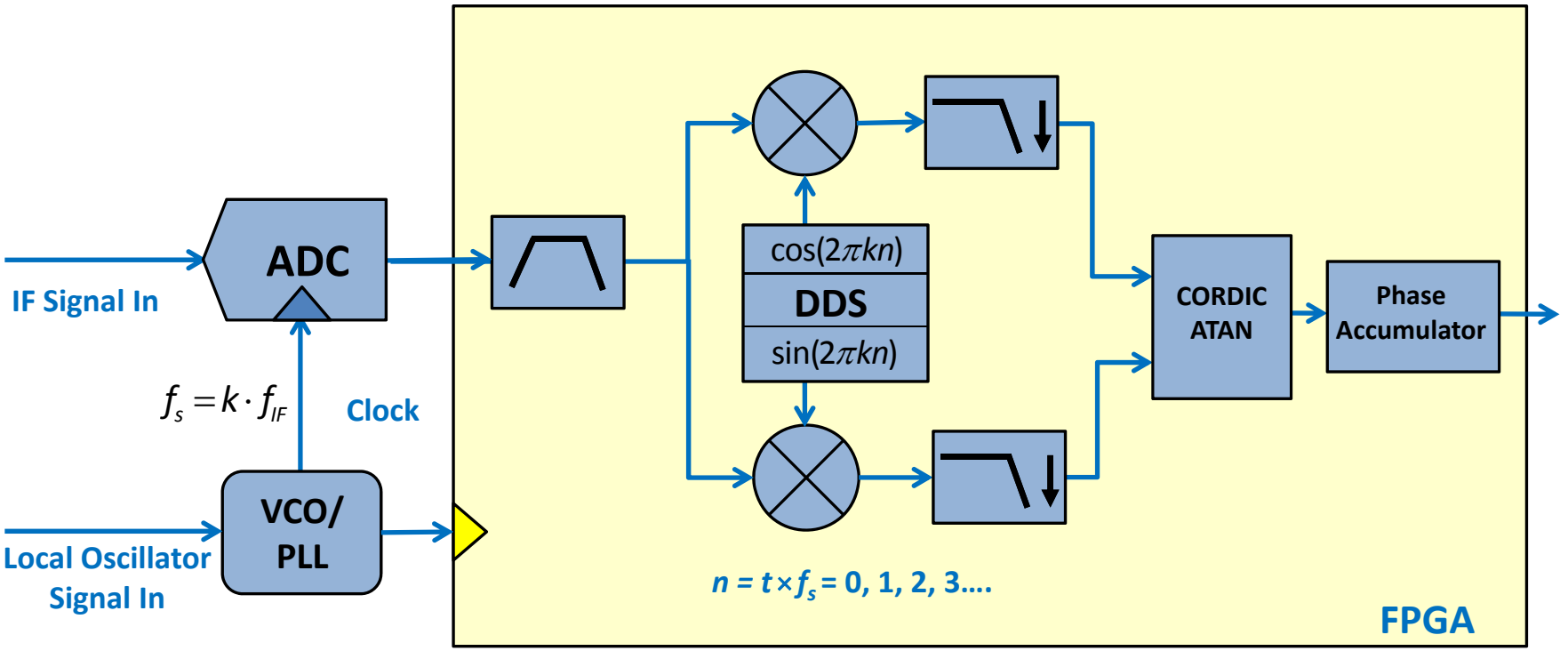


Hi-Frequency terms at 2ω filter out



$$\phi = \tan^{-1}\left(\frac{Q}{I}\right)$$

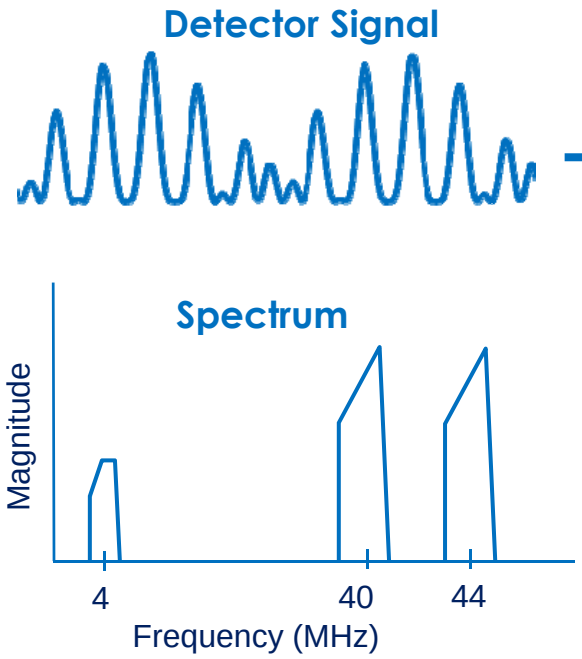
Utilizes Synchronous Sampling and IQ Demodulation

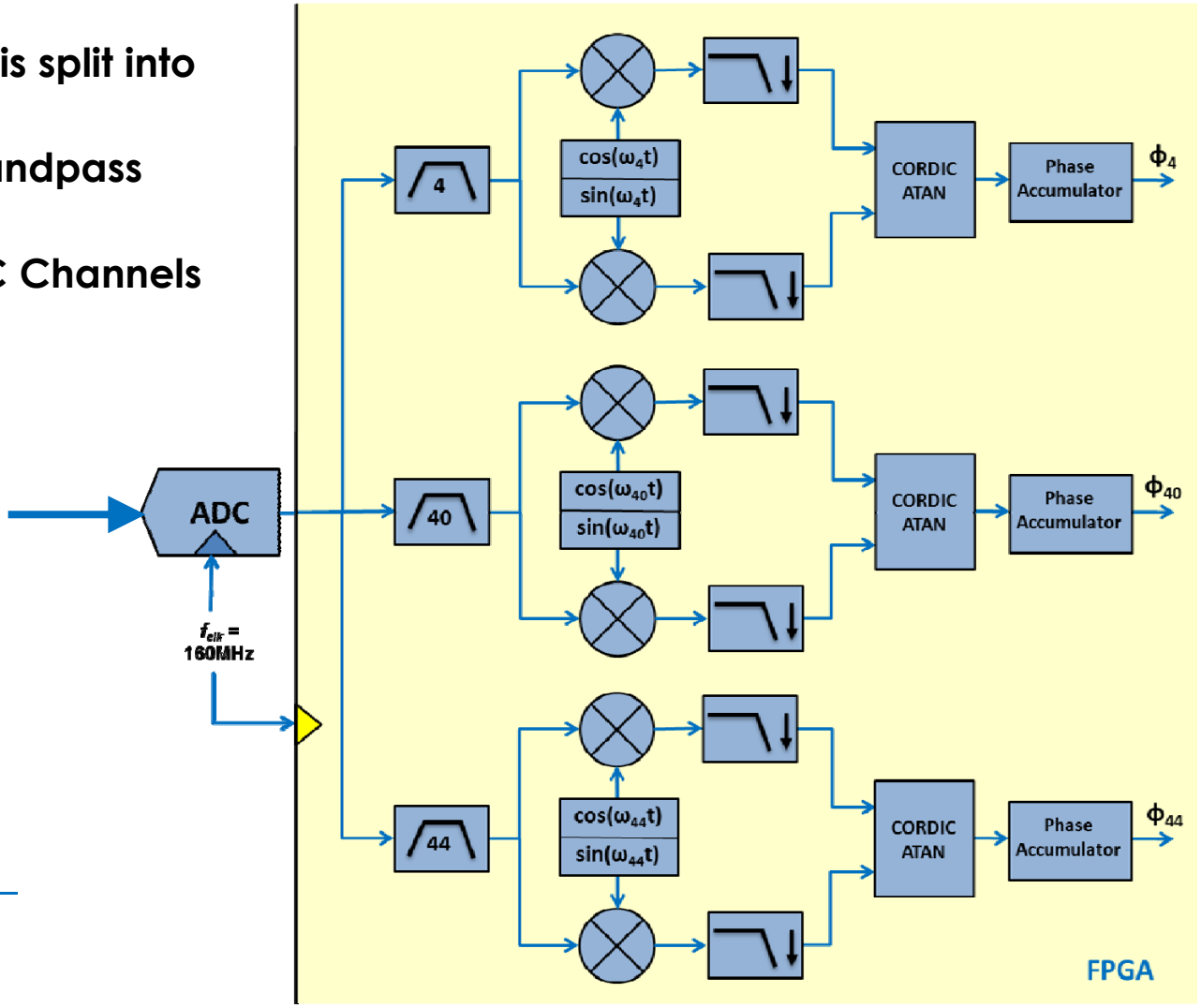


- Clock Tree generates sampling clock synchronized to modulation source Local Oscillator
- Direct Digital Synthesizer (DDS) generates precise sine and cosine reference signals
- Dedicated multipliers are used to mix signals
- FIR Filters used to eliminate high-order mixing products and downsample
- ATAN function implemented using CORDIC (COordinate Rotation Digital Computer)
- Phase accumulator block "unwraps" instantaneous phase limited to ±π

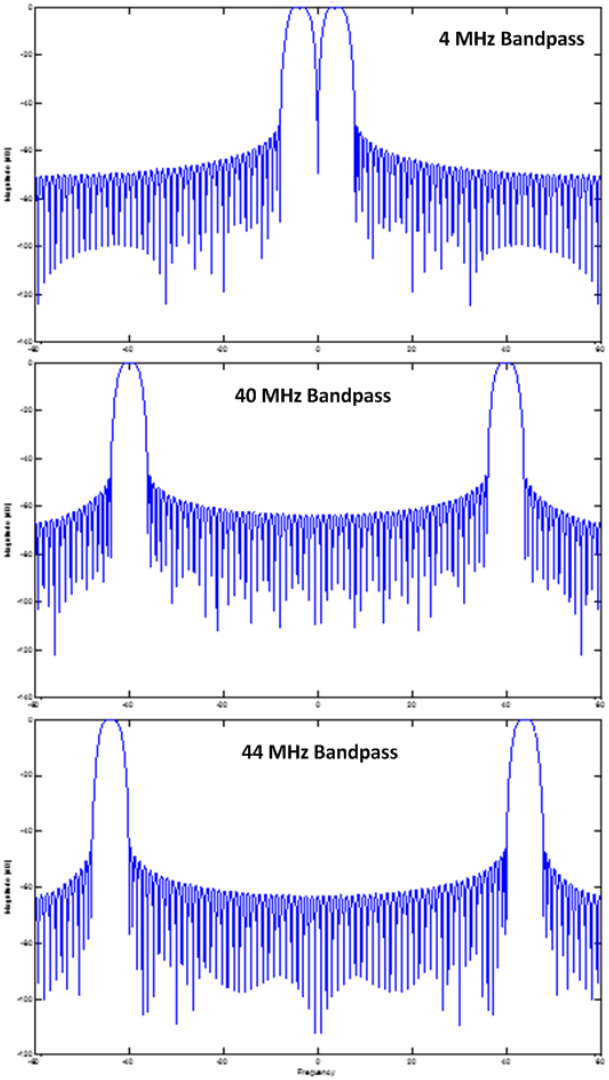
TIP Signals have Three Frequencies to Demodulate

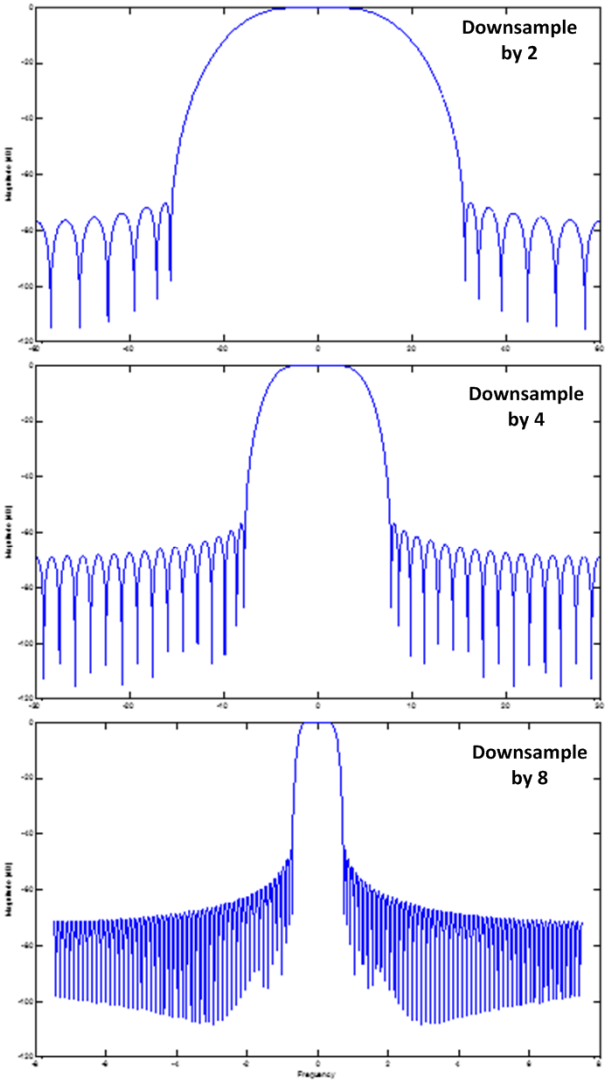
- After sampling the signal is split into 3 Paths
- Each path has strict FIR bandpass filter requirements
- Four Detector signals/ADC Channels total





FIR Filters are used to Separate and Downsample



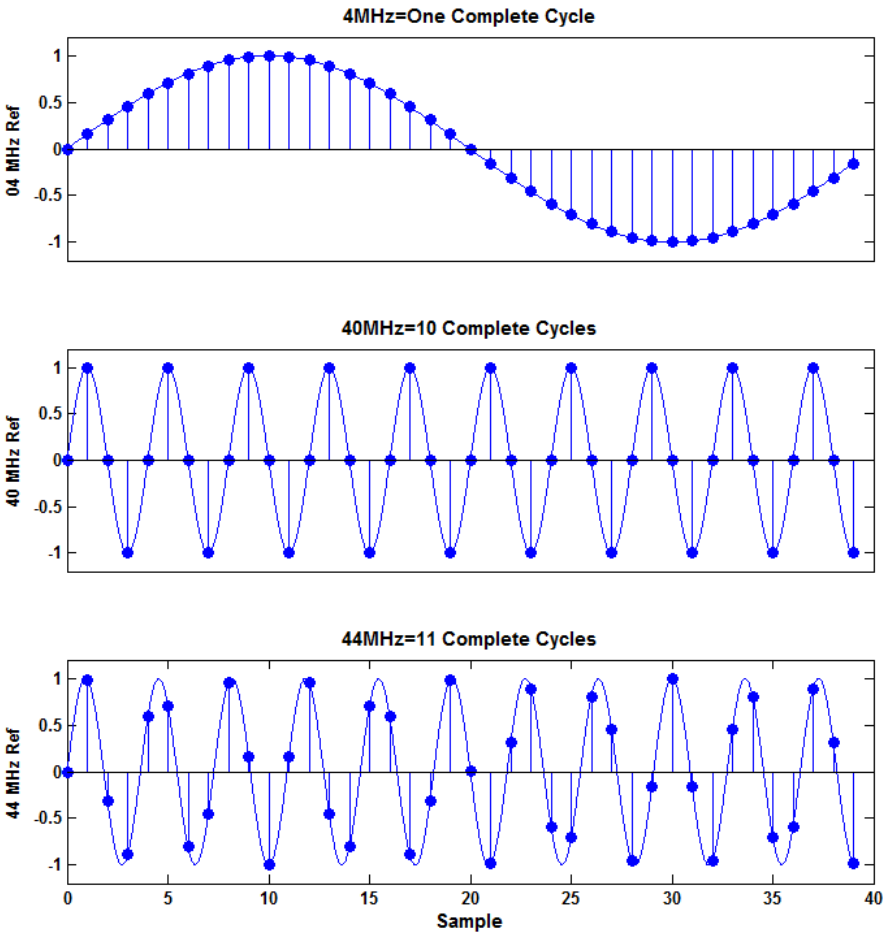


Synchronous Sampling allows mixing with perfect sinusoids

- 4, 40 and 44 MHz reference sinusoids are continuously generated in FPGA
- 40 point look-up table is pre-programmed for 4, 40, and 44 MHZ sine and cosine
- Circular buffer generates
  10 complete 40MHz cycles,
  11 complete 44MHz cycles, and
  1 complete 4MHz cycle
  per buffer
- Possible because of clever choice of IF frequencies (common integer)

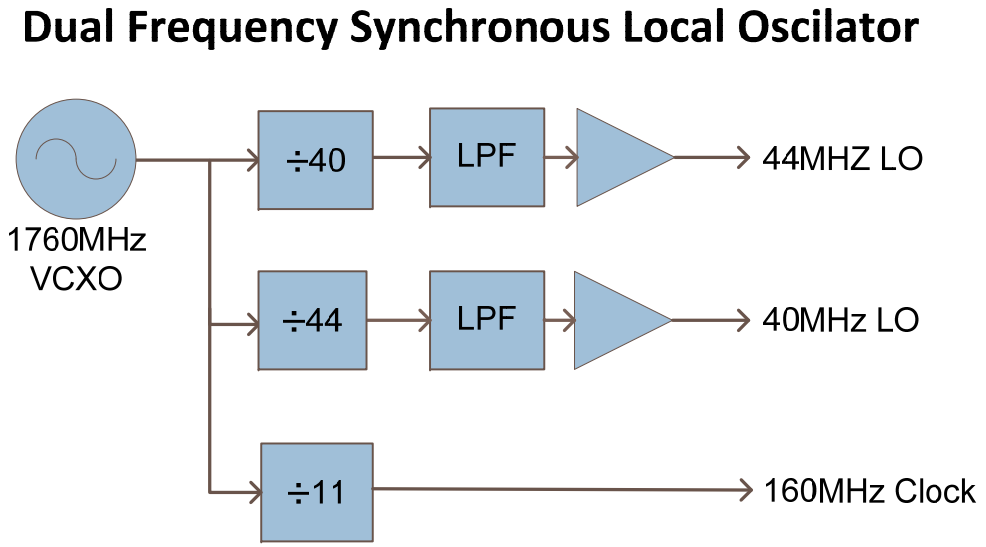
Requires ADC clock be synchronized to IF local oscillator

Reference Sine Functions

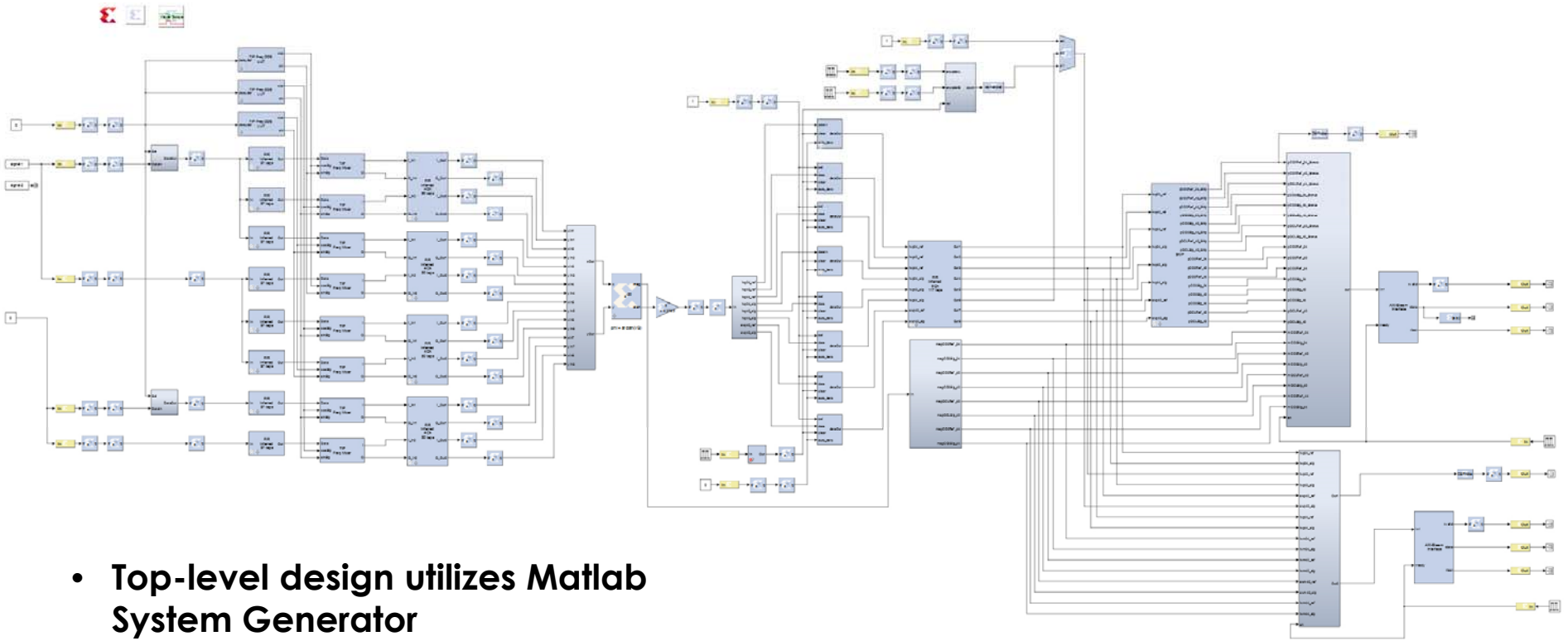


Dual Frequency Synchronous Local Oscillator

- A Single 1760MHz Source is divided down to provide synchronized 40 and 44MHz Local Oscillator (LO) signals
- The 40 and 44MHz LO's each drive an Acousto-Optical Modulator (AOM) to upshift the LH and RH beams
- The 4MHz Polarimeter "Beat" Signal is produced by combining the 40MHz LH and 44MHz RH beams on the optical detector
- All three frequencies are synchronized
- Provides Reference Clock for the Phase Demodulator FPGA



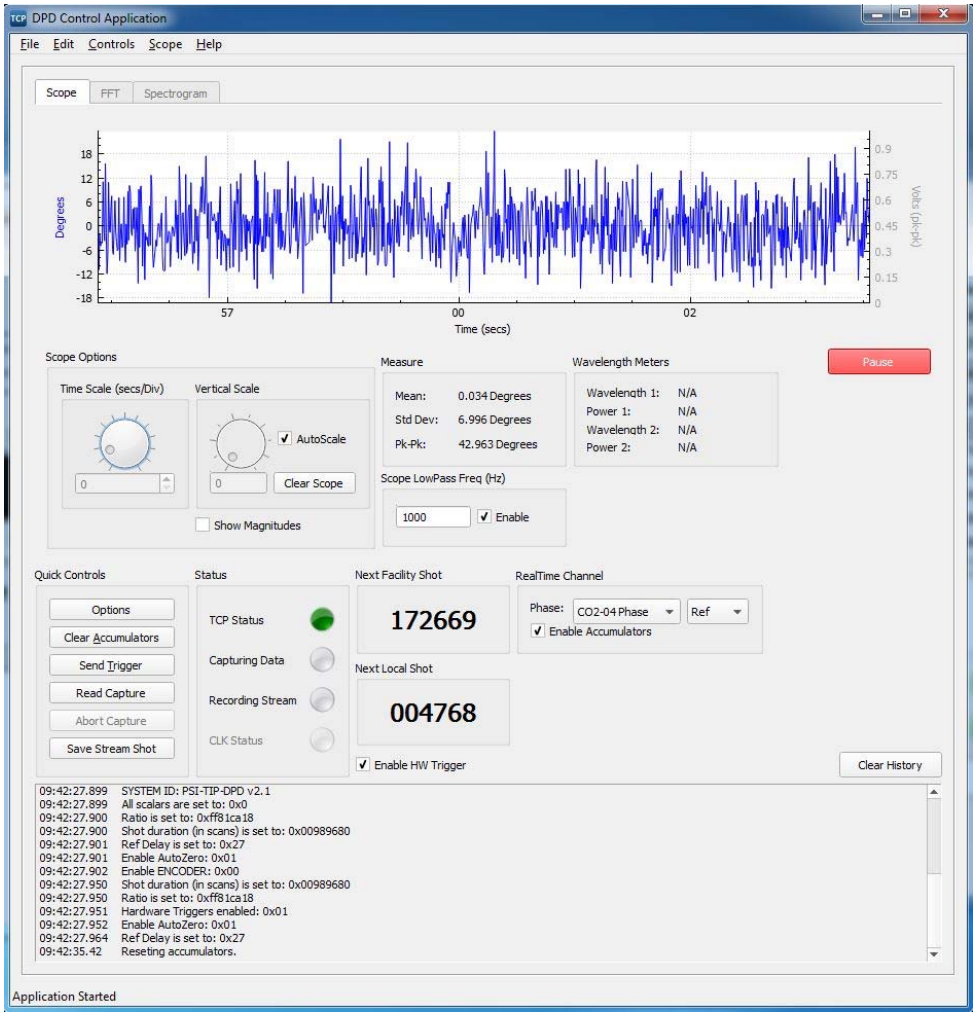
FPGA Development Tools



- **Top-level design utilizes Matlab System Generator**
  - Graphical approach to building effective model.
- **Low-level design done in VHDL**
  - Useful for hardware interfaces, signal manipulation, and efficiency

HMI and Host Software written in C++

- **Provides HMI for monitoring signal phases in Real Time**
  - Crucial for performing highly sensitive optical alignment
- **Provides interface to the Tokamak Plant System including timing and triggering**
- **Uploads data to MDSPlus**
- **Built using QT-toolkit with GCC compiler**
- **Runs on Windows and Linux**



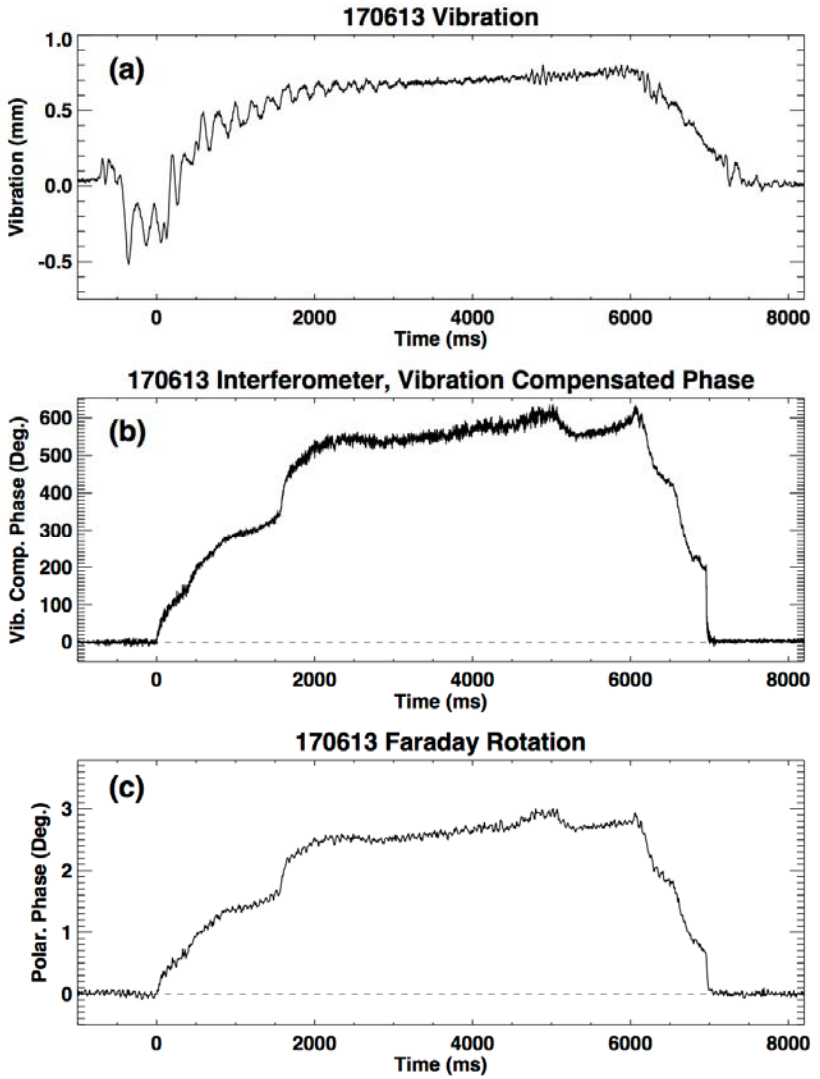
FPGA Device Utilization Summary

Device Utilization Summary (XC7K325T-2FFG900C FPGA)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Registers	79,442	407,600	19%
Number of Look Up Tables (LUT)	64,876	203,800	31%
Number of occupied Slices	26,667	50,950	52%
Number of DSP48E1s	763	840	90%

- **DSP48E1s are dedicated DSP slices**
- **Contain multiply and accumulate (MAC) cells foundational to DSP design**
- **The majority of the MAC cells are used by the FIR logic implementations.**

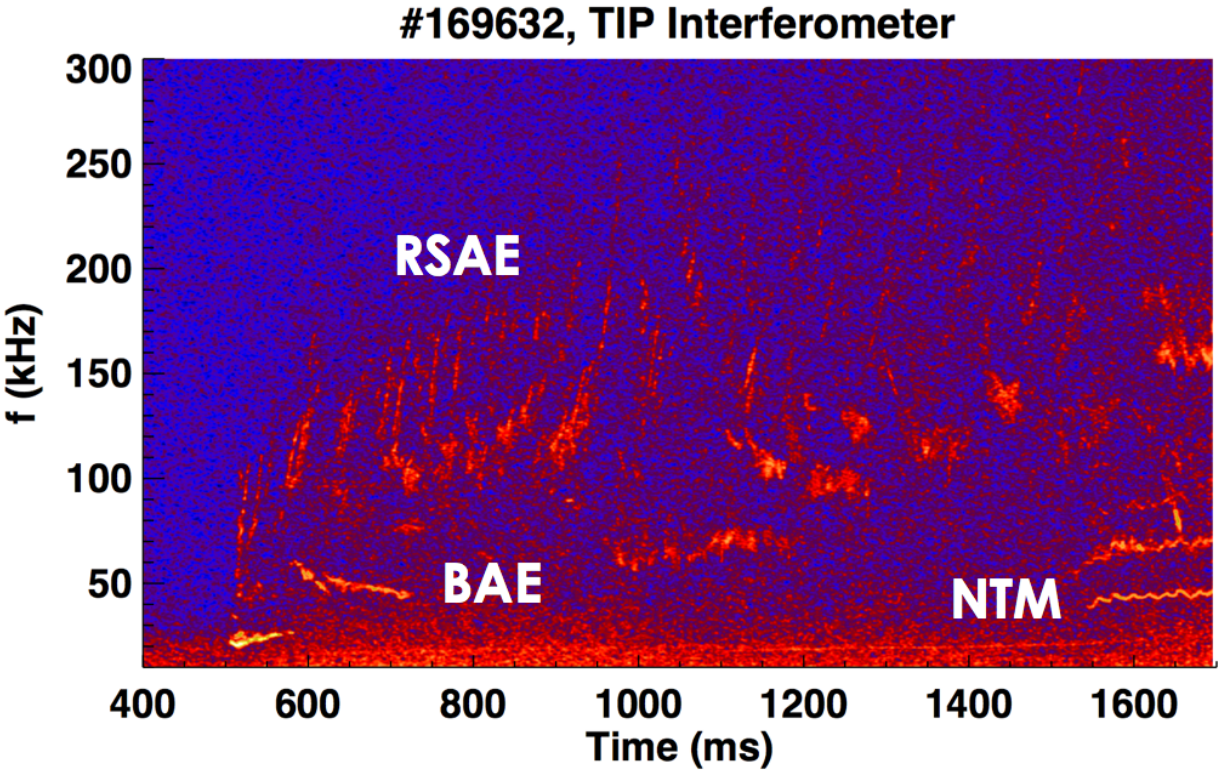
TIP Test Results on DIII-D

- **TIP has been operating on DIII-D for more than year**
  - Includes full-scale mock-up of 120m beam path
- **Routinely Provides Real-Time Density and Faraday Rotation Measurements**
  - Largely Automated
- **Measurements meet ITER Requirements**
- **DIII-D has some bigger challenges**
  - Large Vibrations: each 1mm of machine motion produces a CO2 phase shift of 67,924º
  - Smaller Polarimeter phase shifts



TIP Test Results on DIII-D (Fluctuation Measurements)

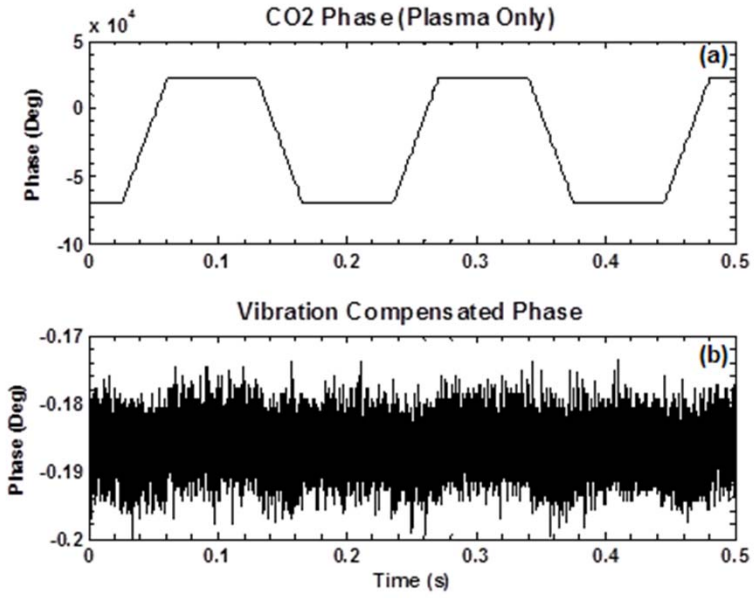
- **TIP Interferometer provides excellent core fluctuation diagnostic**
  - High-Sensitivity
  - High Bandwidth

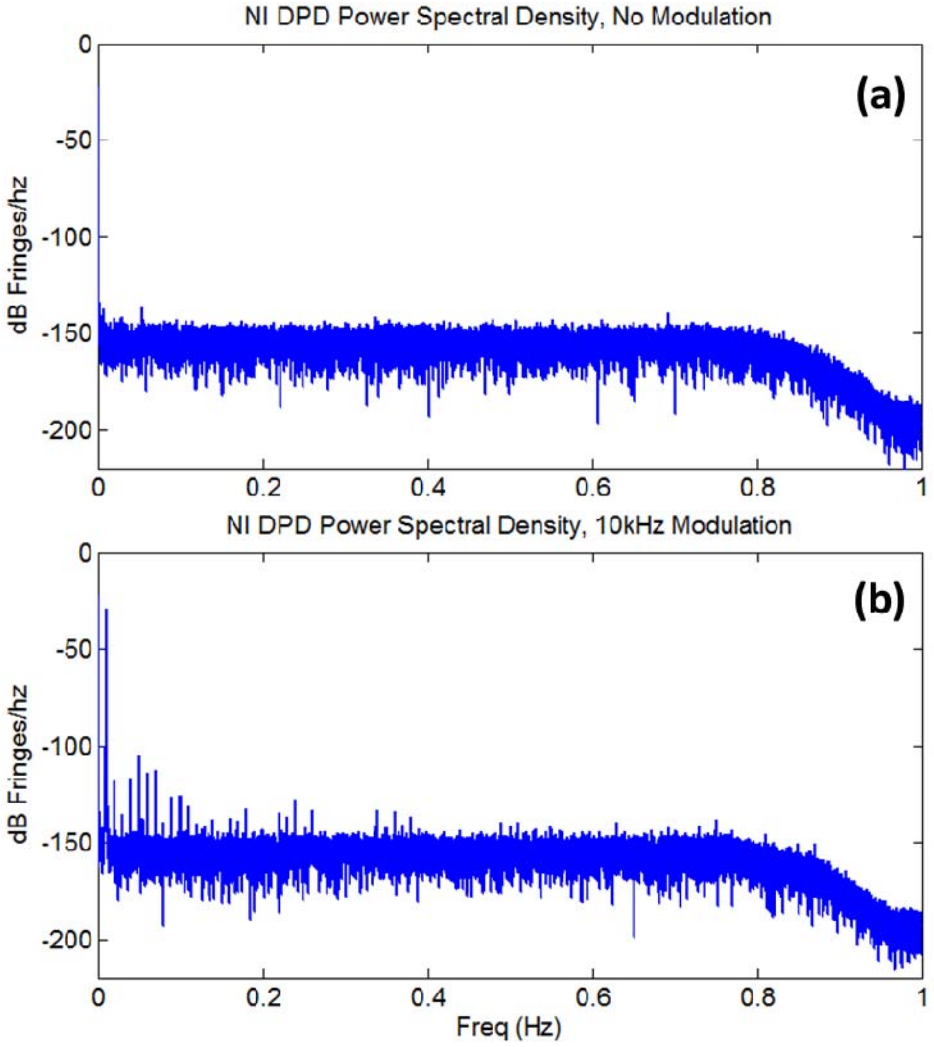


Spectrogram of CO2 Interferometer signal showing coherent mode activity including Beta Induced Alfven Eigenmode (BAE) and the Reversed Shear Alfven eigenmode (RSAE). Neoclassical Tearing Modes (NTM) are also evident (see Van Zeeland's paper)

Accuracy and Noise Floor Measurement

- **FPGA-based "Fringe Generator" constructed using 1GHz DACs**
- **Provides means for testing demodulator accuracy and noise floors**
- **Arbitrary phase profile can be programmed**
- **Trapezoid has been useful**





Digital Phase Demodulator has Extensive Applications

- **DIII-D Vibration Compensated CO2 Interferometer**
  - In operation since 2008
  - Virtex-II generation FPGA
  - Critical Diagnostic
  - Real-Time Plasma Control
- **Dispersion Interferometer (DI)**
  - Visiting Scientist T. Akiyama setup demonstration DI system on DIII-D in June 2016
  - Uses single 40MHz Heterodyne Laser
  - TIP DPD used for Phase measurement
  - Results shown on right
- **Low-Field Side Reflectometry (LFSR)**
  - ITER Preliminary Design Review Scheduled for June 2018

Demonstrates power and flexibility of FPGA-based phase demodulators